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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,383	02/06/2004	Salman Akram	MI22-2469	6354

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EXAMINER	
PERT, EVAN T	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,383	AKRAM ET AL.	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-43 and 53-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,33,37-43,53-55,57,60-62,64,67-73 and 76-83* is/are rejected.

7)☒ Claim(s) *34-36, 56, 58, 59, 63, 65, 66 and 74-75* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *0806, 1206*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species I in the reply filed on December 6, 2006 is acknowledged. The traversal is on the grounds that 1) Species I and Species II are not mutually exclusive, and 2) a serious burden of search has not been evidenced.

This is not found persuasive because Species I and Species II are mutually exclusive (i.e. Species I is sensing temperature of a wafer and Species II is sensing temperature of something that is not a wafer) per the paper mailed November 6, 2006.

Furthermore, serious burden "may be *prima facie* shown by appropriate explanation of separate classification," which was shown to be Class 438 and Class 374, for example. See MPEP 803(II).

While applicant's traversal is not convincing, the examiner did not properly identify generic claims, and so the restriction requirement is none-the-less withdrawn in order to expedite prosecution.

The petition traversing the restriction filed December 6, 2007 is considered moot.

Claims 32-43 and 53-83 are pending for consideration.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 32, 33, 37-43, 53-55, 57, 60-62, 64, 67-73 and 76-83 are rejected under 35 U.S.C. 102(b) as being anticipated by Moslehi (US 5,436,494 cited on IDS #0204).

Regarding claim 32, the '494 reference discloses a method of sensing temperature of an electronic device workpiece comprising: providing an electronic device workpiece (i.e. providing a temperature calibration wafer such as "20" shown in Fig. 3); supporting a temperature sensing device (i.e. sensor 16) using the electronic device workpiece (16 is patterned on the wafer 20); providing an electrical interconnect upon a surface of the electronic device workpiece (i.e. providing feed lines 10, 14 seen as interconnects connecting edge 22 pads and sensors 16 in Fig. 3); electrically coupling the electrical interconnect with the temperature sensing device (i.e. patterning a metallic layer such that interconnects 10, 14 are electrically coupled to sensor element 12 as seen in Fig. 2); and sensing temperature of the electronic device workpiece using the temperature sensing device (col. 4, lines 22-24 and lines 63-68).

Regarding claim 33, the '494 reference discloses wire bonding the electrical interconnect and the temperature sensing device (i.e. the electrical interconnect 10, 14 and the temperature sensing device 12, 16 are wire bonded are effectively both wire bonded at edge 22 pads per col. 6, lines 5-8).

Regarding claim 37, the '494 reference discloses forming the temperature sensing device (i.e. sensor 16 is formed by patterning element 12 on the wafer).

Regarding claim 38, the '494 reference discloses forming a resistance temperature device (element 12 is a resistance temperature device per col. 5, lines 1-13).

Regarding claim 39, the '494 reference discloses electrically coupling the electrical interconnect with external circuitry (col. 6, lines 1-8).

Regarding claim 40, the '494 reference discloses electrically coupling the temperature sensing device with an edge of the electronic device workpiece using the electrical interconnect (as seen in Fig. 3 where edge 22 pads are connected to sensors 16).

Regarding claim 41, the '494 reference discloses that providing the electrical interconnect comprises forming a conductive trace (col. 5, lines 14-16).

Regarding claim 42, the '494 reference discloses contacting the electrical interconnect with the temperature sensing device (i.e. the feed line interconnects 10, 14 are contacted with sensing elements 12 per Fig. 2) .

Regarding claim 43, the '494 reference discloses sensing temperature of the electronic device workpiece comprising a semiconductive wafer (e.g. col. 2, line 16).

Regarding claim 53, the '494 reference discloses a method of sensing temperature of an electronic device workpiece comprising: providing an electronic device workpiece (i.e. providing device workpiece seen in Fig. 3); forming a temperature sensing device over the electronic device workpiece (i.e forming a senor 16 by forming element 12), the forming including providing the temperature sensing device in a temperature sensing relation with the electronic device workpiece (i.e. elements 12 are provided in temperature sensing relationship with the wafer per col. 4, lines 22-68); and sensing the temperature of the electronic device workpiece using the temperature sensing device (e.g. temperature calibration procedure per col. 6).

Regarding claim 54, the '494 reference discloses providing an electrical interconnect upon the electronic device workpiece (i.e. 10, 14); and electrically coupling the electrical interconnect with the temperature sensing device (i.e. 10, 14 are electrically coupled to the ends of the sensor element 12 per Fig. 2).

Regarding claim 55, the '494 reference discloses that providing the electrical interconnect comprises forming a conductive trace (traces 10, 14 seen in Fig. 3 per col. 5, lines 14-16).

Regarding claim 57, the '494 reference discloses that electrically coupling includes contacting the electrical interconnect and the temperature sensing device (i.e. the contacting seen in Fig .2 wherein interconnects 10, 14 are "contacted" with ends of sensor element 12).

Regarding claim 60, the '494 reference discloses that the forming comprises forming a resistance temperature device (12 is a resistance temperature device per col. 5, lines 1-13).

Regarding claim 61, the '494 reference discloses forming plural temperature sensing devices upon the electronic device workpiece (e.g. col. 5, lines 21-34).

Regarding claim 62, the '494 reference discloses a method of sensing temperature of an electronic device workpiece comprising: providing an electronic device workpiece (i.e. providing device workpiece seen in Fig. 3); supporting a temperature sensing device using the electronic device workpiece (i.e. supporting sensors 16 on the workpiece); providing the temperature sensing device in a temperature sensing relation with the electronic device workpiece (i.e. the sensors are on the wafer to sense temperature per col. 5, lines 24-26); providing an electrical interconnect upon a surface of the electronic device workpiece (i.e. 10, 14 on the wfare seen in Fig. 3); and electrically coupling the electrical interconnect with the temperature sensing device (i.e. 10, 14 coupled to element 12 per Fig. 2).

Regarding claim 64, the '494 reference discloses that the coupling comprises contacting the electrical interconnect with the temperature sensing device (per Fig. 2, the interconnects 10, 14 contact ends of sensor element 12).

Regarding claim 67, the '494 reference discloses forming the temperature sensing device upon the electronic device workpiece (i.e. sensor elements 12 form sensors 16 on the wafer seen in Fig. 3).

Regarding claim 68, the '494 reference discloses coupling the electrical interconnect with circuitry external to the electronic device workpiece (col. 6, lines 1-8).

Regarding claim 69, the '494 reference discloses electrically coupling the temperature sensing device with an edge of the electronic device workpiece using the electrical interconnect (seen in Fig. 3, sensors 16 connected to edge 22 pads by interconnects 10, 14).

Regarding claim 70, the '494 reference discloses that the providing the electrical interconnect comprises forming a conductive trace (i.e. forming traces 10, 14).

Regarding claim 71, the '494 reference discloses a temperature sensing method comprising: supporting a temperature sensing device using a wafer (i.e. supporting sensor elements 12 to form sensors 16 supported by wafer seen in Fig. 3); providing the temperature sensing device in a temperature sensing relationship with respect to the wafer (col. 5, lines 24-26); exposing the wafer and the temperature sensing device to process conditions effective to form at least one electronic device (e.g. processing chamber example of Fig. 1 where device workpiece is used as a calibration of emissivity for temperatuire measurements); and sensing a temperature of the wafer using the temperature sensing device during the exposing (i.e. the wafer is used to measure temperature during process conditions effective to form at least one electronic device for calibration of emissivity values per col. 4).

Regarding claim 72, the '494 reference adjusting the process conditions responsive to the sensing (conditions of emissivity values are compensated per col. 4, lines 25-27).

Regarding claim 73, the '494 reference discloses sensing the temperature of the wafer at a plurality of positions covering substantially an entirety of a surface of the wafer (col. 5, lines 24-26).

Regarding claim 76, the '494 reference discloses that providing the electronic device workpiece comprises providing a wafer comprising silicon (e.g. col. 1, line 37).

Regarding claim 77, the '494 reference discloses that the sensing comprises sensing the temperature of the electronic device workpiece during fabrication of an electronic device using the electronic device workpiece (i.e. fabrication flow includes calibration wafer explained at col. 4 so the fabrication includes the calibration using the wafer of Fig. 3).

Regarding claim 78, the '494 reference discloses that providing the electronic device workpiece comprises providing a wafer comprising silicon (e.g. col. 1, line 37).

Regarding claim 79, the '494 reference discloses that the sensing comprises sensing the temperature of the electronic device workpiece during fabrication of an electronic device using the electronic device workpiece (i.e. fabrication process including calibration such that "during fabrication" includes a calibration during the fabrication flow).

Regarding claim 80, the '494 reference discloses that the providing the electronic device workpiece comprises providing a wafer comprising silicon (e.g. col. 1, line 37).

Regarding claim 81, the '494 reference discloses sensing temperature of the electronic device workpiece during fabrication of an electronic device using the electronic device workpiece (i.e. fabrication process including calibration such that "during fabrication" includes a calibration during the fabrication flow).

Regarding claim 82, the '494 reference discloses that the supporting comprises supporting the temperature sensing device using the wafer comprising silicon (e.g. col. 1, line 37).

Regarding claim 83, the '494 reference discloses that the sensing the temperature comprises sensing the temperature of the wafer during fabrication of an electronic device using the wafer workpiece (i.e. fabrication process including calibration such that "during fabrication" includes a calibration during the fabrication flow).

Allowable Subject Matter

4. Claims 34-36, 56, 58, 59, 63, 65, 66 and 74-75 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: The prior art discloses a temperature sensor provided within a cavity of a wafer (e.g. Fig. 5 of US 5,969,639), yet the prior art fails to suggest the claimed combination of forming a temperature sensing device in a cavity while also forming interconnects for the temperature sensing device upon a surface of the wafer such that the sensing can comprise sensing temperature in three dimensions of the wafer.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US 6,190,040 is cited for disclosing temperature sensors and interconnects deposited directly on a wafer (col. 8 line 29 to col. 11), yet fails to disclose forming a cavity for the temperature sensing device, such as by anisotropic or isotropic etching.

US 6,037,645 is cited for disclosing thermocouples deposited directly on a wafer along with interconnects, yet fails to disclose a cavity for a thermocouple to be formed in.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EVAN PERT
PRIMARY EXAMINER

ETP
March 31, 2007